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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER
PHILPOTT, JUSTIN M

ART UNIT	PAPER NUMBER
2665	13

DATE MAILED: 08/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/242,822	Applicant(s) FICHE, GEORGES	
	Examiner Justin M Philpott	Art Unit 2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 June 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☒ The proposed drawing correction filed on *28 December 2002* is: a)☒ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Continued Prosecution Application

1. The request filed on June 4, 2003 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/242,822 is acceptable and a CPA has been established. An action on the CPA follows.

Response to Amendment

2. In the Amendment filed April 25, 2003, Applicant has amended the specification to clarify Figures 4A and 4B such that Figure 4B is no longer required to be designated by a legend such as --Prior Art--. Accordingly, the specification is no longer objected to. Applicant has also amended claim 1 to recite further limitations and has argued that the cited prior art does not teach such limitations.

Response to Arguments

3. Applicant's arguments (pages 4-11) with respect to claims 1-5 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 103

4. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims 1 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong in view of U.S. Patent No. 5,642,349 to Cloonan et al.

Regarding claim 1, Wong teaches devices for switching ATM cells (figures 1-4; primary reference is made to the general architecture of figure 1 which figures 2- 4 are based upon) establishing a single path per virtual circuit having N.R inputs (k.n inputs) and N.R outputs (l.p outputs), N and R (k or l, and n or p) being two integers not less than two, the device comprising at least two stages, including an inlet stage (n x m stage) comprising a plurality of matrices (1 to k) and having R.N sets (n.k sets) of Q outputs (r) and an outlet stage (s x p stage) comprising a plurality of matrices (1 to *l*) and having R.N sets (p.l sets) of Q' inputs (r) – wherein n=p, m=n, and m=s (see page 709, col. 1, lines 4 and 17) and wherein figures 1 and 2 indicate k=l, thus, n=m=s=p=R and k=l=N. Furthermore, the above is characterized in that for the flow of data carried by any intermediate link (one of the links in a grouping of r links, see page 708, column 2) that is part of the single path set up between an input and an output (r) to be a subset of the incoming flux at that input and also a subset of the outgoing flux at that output, each input (n) of the inlet stage (n x m stage) can be connected to an output of the inlet stage (at m, one of the lines of a corresponding grouping of r lines) which can be selected only from Q outputs (r lines) associated with that input (e.g., r lines are provided "for each path between the two stages"); and in that each output (p) of the outlet stage (s x p stage) can be connected to an input of the outlet stage (at s, one of the lines of a corresponding grouping of r lines) which can be selected only from Q' inputs (r lines) of the output stage associated with that output (p). However, Wong may not specifically disclose an exclusive association between each inlet stage input/outlet stage

output and each set of Q outputs/Q' inputs (r lines) such that the flow of data at each input of the inlet stage can be directed to each matrix of the outlet stage.

Cloonan teaches an improvement for packet switching, and specifically, teaches improvements over Clos and Banyan multistage networks (e.g., see col. 4, lines 20-64) such as those taught by Wong. Specifically, Cloonan teaches a switch device (e.g., 10A in FIG. 4) wherein each inlet stage input (e.g., In_0 - In_{N-1}) is exclusively associated with Q outputs of the inlet stage (e.g., 17_0 comprising connections to each $PIPE_{0-3}$) and each outlet stage output (e.g., 0-255 of modules 16_{0-15}) is associated with Q' inputs of the outlet stage (e.g., links of 17_{0-255} via $PIPE_{0-3}$). The teachings of Cloonan provide an improved ATM switch with lower cell loss probability than packet switches utilizing Clos and Banyan multistage networks such as those taught by Wong (e.g., see col. 4, lines 60-64). Thus, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the teachings of Cloonan to the switching device of Wong in order to provide lower cell loss probability.

Additionally, while Cloonan uses an example (FIG. 4) of sixteen output modules coupled to four pipes (i.e., Q equal to four), Cloonan further teaches that more than four pipes may be utilized (e.g., see col. 20, lines 59-67), wherein, e.g., additional hardware would be required, and Cloonan also teaches that other combinations of components can be used including a different number of output modules (e.g., see col. 7, lines 23-28). Cloonan also shows a chart (FIG. 9) which indicates an improvement in cell loss probability with an increased number of pipes. Thus, for applications having less stringent hardware limitations, the teachings of Cloonan suggest a switch device having additional pipes (e.g., eight, sixteen, etc.). Such a device would also clearly provide for the flow of data at each input of the inlet stage (e.g., In_0 - In_{N-1}) to be

directed to each matrix (e.g., modules $16_{0\text{-}15}$) of the outlet stage (wherein the number of pipes and output modules are, e.g., sixteen) thereby exclusively associating each output of the output modules with Q' inputs. At the time of the invention it would have been obvious to one of ordinary skill in the art to utilize a greater number of pipes, such as sixteen, in the switch device of Cloonan as suggested by Cloonan by teaching that more than four pipes may be utilized and by teaching that cell loss probability improves with additional pipes.

Regarding claim 4, Wong teaches (figure 3) an inlet stage (n x m stage), a central stage (l x l' stage), and an outlet stage (m' x n' stage) characterized in that Q and Q' (r and r') are equal to R (e.g., see page 709, col. 2, line 17 and page 710, col. 1, line 10 wherein l=l' and m=m' and therefore r=r'=(Q=Q')=m=R), the central stage (l x l' stage) includes R^2 matrices (r=r', therefore the l x l' stage includes r^2 or R^2 matrices), and the matrices of the inlet stage and the matrices of the central stage are organized into R sets (n sets) each including N matrices (h matrices) of the inlet stage and R matrices (g matrices, where g may be equal to m) of the central stage and the matrices of the outlet stage are organized into N sets (h' sets) of R matrices (m' matrices, where m' may equal r'). Furthermore, the above is characterized in that each of the R.N matrices of the inlet stage (n x m stage) has a single input (i.e., the first/top input at n) and R outputs (r lines), each of the R^2 matrices of the central stage has N inputs and N outputs (l inputs and l' outputs) – the inputs being respectively connected to an output of each of the matrices of the inlet stage that belong to the same set of matrices, and each of the R.N matrices of the outlet stage (m' x n' stage) has R inputs (r' lines) and a single output (i.e., the first/top output at n'), those R inputs (r' inputs) being connected to outputs respectively belonging to the R sets of matrices of the central stage and of the inlet stage.

6. Claims 2, 3 and 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong in view of Cloonan, further in view of U.S. Patent No. 5,467,347 to Petersen.

Regarding claim 2, Wong in view of Cloonan teaches the device described with the exception that Wong in view of Cloonan may not specifically disclose each matrix having exactly R.N outputs (n.k outputs) organized into R sets (n sets) of N outputs (k outputs) with each set corresponding to a respective one of the R inputs (n inputs). Petersen teaches improvements for ATM switching means wherein an inlet stage (e.g., switchport 11, see FIG. 1) is coupled to a plurality of outlet stages (e.g., switchcore 12 having planes a and b) wherein each matrix of the inlet stage (e.g., switchport 11) has outputs organized into a number of sets (one in this example) of N (n) outputs (n=2 in this example). Applying this configuration of Petersen to an ATM switching device allows for implementation on a single chip and greatly reduces hardware and maintenance costs while increasing reliability (see col. 5, lines 20-35). Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the ATM switching arrangement of Petersen to the ATM switching device of Wong in view of Cloonan in order to reduce cost and increase reliability.

Regarding claim 3, Wong teaches (figure 2) an inlet sage (n x m stage), a central stage (k x k stage), and an outlet stage (m x n stage) characterized in that, Q being equal to R (n), the inlet stage comprises N (k) matrices each having R (n) inputs each of which can be connected to an output of that matrix which can be selected only from R (m, or n wherein m=n; see page 709, col. 1, line 17) outputs of the set of outputs corresponding to that input, and the central stage (k x k) comprises a set of R (m) matrices each having N (k) inputs and N (k) outputs wherein the R

(m) outputs of each set of outputs of the inlet stage are connected to inputs belonging to the same set of R (k) matrices of the central stage. Furthermore, the above is characterized in that, Q' being equal to R (n), the outlet stage comprises N (k) matrices each of which have R (m) inputs and R (n) outputs, wherein each output of a matrix can be connected to an input of that matrix which can be selected only from R (m) inputs corresponding to that output. However, as with claim 2 above, Wong in view of Cloonan may not specifically disclose each matrix having inputs/outputs organized into R sets of R inputs/outputs and, similarly, may not specifically teach each matrix of the inlet stage has R^2 outputs, or R sets of R outputs, and likewise may not teach R sets of R matrices in the central stage or R^2 inputs in each matrix of the outlet stage. As discussed above, Petersen teaches improvements for ATM switching means wherein the inlet stage (switchport 11) has R^2 outputs, or b sets of n outputs (wherein b=2 and n=2, in FIG. 1). Such an arrangement reduces cost and increases reliability and can be advantageously applied to the device taught by Wong in view of Cloonan to provide these improvements. Having R^2 outputs in the inlet stage, the device of Wong in view of Cloonan further in view of the teachings of Petersen would further comprise R sets of R matrices in the central stage and similarly R^2 inputs in each matrix of the outlet stage in order to provide the desired ATM switching taught by Wong in view of Cloonan with the improvements in ATM switching taught by Petersen. Therefore, at the time of the invention it would have been obvious to one of ordinary skill in the art to apply the ATM switching teachings of Petersen to the ATM switching device of Wong in view of Cloonan in order to provide a more robust ATM switching device with reduced cost and increased reliability.

Regarding claim 5, the device of Wong in view of Cloonan further in view of Petersen teaches a switching device according to claim 3 as discussed above. Furthermore, such a device having three stages may advantageously be implemented with N and R values such that $N=2.R^2$.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

U.S. Patent No. 5,506,840 to Pauwels et al. discloses a switching fabric having an inlet stage and outlet stage whereby the flow of data at each input of the inlet stage can be directed to each matrix of the outlet stage (e.g., see FIG. 3), and

U.S. Patent No. 6,188,690 to Holden et al. also discloses a switching fabric having an inlet stage and outlet stage whereby the flow of data at each input of the inlet stage can be directed to each matrix of the outlet stage (e.g., see switch card in FIG. 5).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Justin M Philpott whose telephone number is 703.305.7357. The examiner can normally be reached on M-F, 9:00am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy D Vu can be reached on 703.308.6602. The fax phone numbers for the organization where this application or proceeding is assigned are 703.872.9314 for regular communications and 703.872.9314 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703.305.4750.

Justin M Philpott

August 6, 2003

HUY D. VU
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